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**B.TECH.**  
**(SEM VII) THEORY EXAMINATION 2019-20**  
**VLSI DESIGN**

Time: 3 Hours

Total Marks: 70

Note: Attempt all Sections. If require any missing data; then choose suitably.

**SECTION A**

1. Attempt *all* questions in brief. 2x7=14
- a) What do you mean by  $Z_{pd}$ ,  $Z_{pl}$  in the inverter circuit.
  - b) Give the circuit arrangement for 2 input NOR gate using CMOS logic.
  - c) What is parasitic delay.
  - d) What is channel length modulation
  - e) Implement 2:1 MUX using CMOS Transmission Gate.
  - f) What are needs for low power VLSI chips.
  - g) Write down the Applications of FPGA.

**SECTION B**

2. Attempt any *three* of the following: 7x3=21
- (a) Explain the Fabrication Process of N-MOS transistor. Explain the MOSFET capacitance with suitable sketch.
  - (b) Derive the expression for  $V_{IH}$ ,  $V_{IL}$ ,  $NM_L$ , and  $NM_H$  for CMOS inverter.
  - (c) Explain Domino and NORA CMOS logic circuit with suitable example.
  - (d) Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells.
  - (e) Explain the following:
    - (i) Scan Based Technique.
    - (ii) Fault types and models.

**SECTION C**

3. Attempt any *one* part of the following: 7x1=7
- (a) Discuss the hierarchy of various semiconductors with Moore's law. Draw the Y- chart and explain the VLSI design process.
  - (b) Implement the Boolean function  $Z = AB + (C + D)(E + F) + GH$  using standard CMOS and Domino CMOS logic.
4. Attempt any *one* part of the following: 7x1=7
- (a) Why transistor scaling is of great importance in VLSI? Write down comparison between Constant field scaling and Constant voltage scaling. <https://www.aktuonline.com>
  - (b) (i) Explain the concept of RC Delay model.  
(ii) What are the limitations of logical effort.
5. Attempt any *one* part of the following: 7x1=7
- (a) Draw the circuit diagram of SRAM and explain read and write operation.
  - (b) Explain various types of power dissipation in CMOS circuits.
6. Attempt any *one* part of the following: 7x1=7
- (a) Write the Difference between Dynamic CMOS logic circuit and Static CMOS logic circuit. Explain the classification of Dynamic CMOS logic circuit and design a 2 input EXOR logic Gate using Domino logic.
  - (b) Describe the working of three stage pseudo nMOS dynamic shift register driven with two-phase clocking giving its circuit.
7. Attempt any *one* part of the following: 7x1=7
- (a) Write a short note on Built-in-self test (BIST) techniques.
  - (b) Briefly explain variable threshold CMOS (VTCMOS) circuit.