

**B. TECH**  
**(SEM-VII) THEORY EXAMINATION 2018-19**  
**VLSI DESIGN**

*Time: 3 Hours**Total Marks: 100***Note:** 1. Attempt all Sections. If require any missing data; then choose suitably.**SECTION A**

- 1. Attempt *all* questions in brief. **2 x 10 = 20****
- a. Why we need a low power VLSI circuits in today's scenario?
  - b. Explain the terms packaging and testing.
  - c. Define logical effort with example.
  - d. Define the terms- Defects, Errors and Faults.
  - e. Distinguish between SRAM and DRAM.
  - f. Bring out the drawbacks of dynamic logic.
  - g. Explain the term controllability and observability.
  - h. Why we prefer CMOS transmission gates over other gates?
  - i. Define the term Interconnect.
  - j. What is meant by Stuck-at-1(s-a-1) fault and Stuck-at-0(s-a-0) faults.

**SECTION B**

- 2. Attempt any *three* of the following: **10 x 3 = 30****
- a. Illustrate the n-well CMOS fabrication process with neat diagrams.
  - b. Explain the Elmore Delay Model with suitable diagram.
  - c. Write short note on:
    - (i) Logical Effort
    - (ii) Parasitic Delay
  - d. Enlist the advantages of dynamic logic circuit over static logic circuit. Explain NORA CMOS logic circuit with suitable example.
  - e. Describe leakage power dissipation and dynamic power dissipation.

**SECTION C**

- 3. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) (i) Write short note on VLSI testing.  
(ii) Draw and explain the VLSI design Flow(Y-chart).
  - (b) Draw and explain the working of CMOS inverter with its transfer characteristics.
- 4. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) Analyze the Linear delay model with its different limitations.
  - (b) Explain the following circuits:
    - (i) Variable threshold CMOS circuits
    - (ii) Multiple threshold CMOS circuits
- 5. Attempt any *one* part of the following: **10 x 1 = 10****
- (a) Draw and explain the working of Lumped RC-model for interconnects.
  - (b) Explain the Delay Estimation with different optimization techniques.

6. Attempt any *one* part of the following: 10 x 1 = 10
- (a) Explain read/write operation of SRAM memory cell. How 1-bit cell is used in bigger memory systems.
  - (b) (i) Implement the Boolean function  $Y = AB + (C+D)(F+E)+GH$  using DOMINO CMOS logic.  
(ii) Explain the term Voltage Boot Strapping in CMOS logic with suitable examples.
7. Attempt any *one* part of the following: 10 x 1 = 10
- (a) Explain the issues involved in Built-in Self Test (BIST) techniques in detail.
  - (b) (i) Write a short note on Adiabatic Logic Circuit.  
(ii) Explain the Scan Based Techniques.