Subject Code: KEC072

PAPER ID-410415

Roll No: | | | | | | | | | | | | | |

B TECH.
(SEM VII) THEORY EXAMINATION 2021-22
VLSI DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 10 = 20

Qno.	Question	Marks	CO
a.	What is Photolithography?	2	1
b.	Why we need a low power VLSI circuits in today's scenario?	2	1
c.	What is contamination delay?	2	2
d.	Define logical effect with example.	2	2
e.	Differentiate between static power and dynamic power.	2	3
f.	Implement 2:1 MUX using CMOS transmission gate.	2	3
g.	Describe different storage elements.	2	4
h.	Distinguish between SRAM and DRAM.	2	4
i.	Explain the term controllability and observability.	2	5
j.	What is meant by Stuck-at-1 fault and Stuck-at-0 fault?	2	5

SECTION B

2. Attempt any *three* of the following:

Qno.	Question	Marks	CO
a.	Discuss the hierarchy of various semiconductors with Moore's law. Write short note on VLSI testing.	10	1
b.	Explain Elmore delay model with suitable RC networks. Mention its merits.	10	2
c.	Compare the performance of Domino CMOS logic and NP Domino CMOS logic with suitable example.	10	3
d.	Explain read/ Write operation of SRAM memory cell. How 1 bit cell is used in bigger memory systems.	10	4
e.	Explain the issues involved in BIST techniques in details.	10	5

SECTION C

3. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Draw the Y-chart and explain VLSI design process. Mention its advantages.	10	1
b.	Explain the CMOS fabrication steps with neat diagram using n-well process.	10	1

4. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Derive the expression for total power dissipation of a CMOS circuit.	10	2

b.	Draw and explain the working of RC delay model for interconnects.	10	2

5. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Draw and explain NORA and TSPC dynamic CMOS logic.	10	3
b.	What is pre-charge evaluate logic in dynamic CMOS logic and draw the basic architecture of SRAM and DRAM.	10	3

6. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Write short note on DRAM cell. Explain leakage and refresh operation in DRAM cells.	10	4
b.	Explain the various types of power dissipation in CMOS circuits.	10	4

7. Attempt any *one* part of the following:

Qno.	Question	Marks	CO
a.	Explain the parallel procession approach in low power CMOS circuits.	10	5
b.	Write a short note on i. Adiabatic logic circuits ii. Scan cell based approach.	10	5