B TECH
(SEM V) THEORY EXAMINATION 2018-19
INTEGRATED CIRCUITS

Time: 3 Hours   *Total Marks: 100*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. **Attempt *all* questions in brief**   **2 x 10 = 20**
    a. What is improving Wilson current mirror?
    b. What is GIC?
    c. What are the differences between flip flop and latch?
    d. What are the reasons for the offset current at the input of op amp?
    e. Implement F = (xy+x'y')' using AND-OR invert logic.
    f. Define capture range of a PLL.
    g. What is hysteresis voltage?
    h. What are the differences between ADC and DAC?
    i. What is V_{IH} and V_{IL} in CMOS? Explain.
    j. What are the limitations of analog integrated circuits?

SECTION B

2. **Attempt any *three* of the following:**   **10 x 3 = 30**
    a. With the help of neat diagram discuss the problems associated for realizing the beta compensated current mirror using MOS. Also write the differences between base current compensated current mirror and simple current mirror circuit. Explain with the help of neat diagram.
    b. Draw and explain the circuit for the KHN filter using three op amplifier and derive the expression for its voltage gain.
    c. With the help of neat diagram discuss the basic concept of CMOS NOR gate and CMOS NAND gate. Also design a full adder circuit with inputs A, B and C and two outputs S and Ca.
    d.   What is phase detector? What is the main function of phase detector? Briefly describe the various types of phase detectors with circuit diagram and input – output waveform.
    e. Draw and explain the functional block diagram of IC 555. What is the operation of this IC? Design astable multivibrator with an output signal frequency of 500 Hz and 50% duty cycle.

SECTION C

3. **Attempt any *one part* of the following:**   **10 x 1 = 10**

    a. Define the following parameters of op amp.
        (i)   Slew rate
        (ii)   CMRR
        (iii)   Bias current

        Also derive a relationship between f_t and slew rate of an op amp.

    b. With the help of analytical steps explain the Antonion inductance simulation circuit with properly labeled diagram.

4. **Attempt any *one part* of the following:**   **10 x 1 = 10**

    a. With the help of neat diagram explain the basic circuits of voltage to current converter and current to voltage converter using op amp.Also explain the frequency response of op amp IC 741.

    b. What are the differences between active and passive filters? Design a wide BPF with lower cut off frequency f_L= 400Hz, higher cut off frequency f_H = 2000Hz and a pass band gain of 8.

5. **Attempt any *one part* of the following:**   **10 x 1 = 10**

    a. With the help of neat diagram discuss the construction, working principle and characteristics of CMOS inverter. Also derive the V_{IL} and V_{IH} of CMOS inverter.

    b. What are the differences between CMOS SR flip flop and master slave D flip flop circuit. With the help of neat sketches explain the operation of master slave D flip flop circuit.

6. **Attempt any *one part* of the following:**   **10 x 1 = 10**

    a. How can you generate the triangular and square waveform from astable multivibrator. Derive an expression for the time period for both types of waves.

    b. Explain the following with circuit diagrams:

        (i)   Precision rectifier
        (ii)   Zero crossing detector
        (iii)   Sample and hold circuit
        (iv)   Analog multipliers and their applications

7. Attempt any *one part* of the following: **10 x 1 = 10**

    a. Draw the circuit of a 4 bit binary weight D/A converter. Also with the help of neat diagram explain the working of dual slope integrating ADC.
    b. Draw the block diagram of a PLL and explain the function of each block. What are the advantages, disadvantages and applications of PLL. Explain any one application of PLL along with its circuit diagram.