



PAPER ID-411537

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Subject Code: KOE039

Roll No:

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**BTECH**  
**(SEM III) THEORY EXAMINATION 2021-22**  
**DIGITAL ELECTRONICS**

**Time: 3 Hours****Total Marks: 100****Notes:**

- Attempt all Sections and Assume any missing data.
- Appropriate marks are allotted to each question, answer accordingly.

SECTION-A	Attempt <b>All</b> of the following Questions in brief	Marks(10X2=20)	CO
Q1(a)	How are binary digits used to express the integer and fractional parts of a number?		1
Q1(b)	Explain how BCD addition is carried out.		1
Q1(c)	Implement a 4:1 multiplexer using 2:1 multiplexer.		2
Q1(d)	Demultiplexer is decoder circuit with an additional enabling input. Do you agree with the above statement?		2
Q1(e)	Give the difference between positive and negative edge triggering.		3
Q1(f)	A flip-flop has 5 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate reliably?		3
Q1(g)	Define critical race and non-critical race.		4
Q1(h)	What is the significance of state assignment?		4
Q1(i)	Why is ECL logic faster than TTL?		5
Q1(j)	Compare static RAM and dynamic RAM.		5

SECTION-B	Attempt <b>ANY THREE</b> of the following Questions	Marks(3X10=30)	CO
Q2(a)	Realize a 3-input gate using 2-input gates for the following gates: (i) AND (ii) OR (iii) NAND (iv) NOR		1
Q2(b)	(i) Implement a full subtractor circuit using only NAND gates. (ii) Using 4:1 multiplexers, implement the following function $F(A, B, C) = \sum m(0, 2, 3, 5, 7)$		2
Q2(c)	Define bi-directional shift register. Draw and explain 3 bit bi-directional shift register using D flip-flop.		3
Q2(d)	Design a primitive state diagram and state table for a circuit with two asynchronous inputs (X and Y) and one output Z. This circuit is to be designed so that if any change takes place on X and Y, Z is to change states. Assume initially that the two inputs never change simultaneously.		4
Q2(e)	(i) Write a note on interfacing TTL with CMOS. (ii) Explain the parameters used to characterize logic families.		5

SECTION-C	Attempt <b>ANY ONE</b> following Question	Marks (1X10=10)	CO
Q3(a)	Minimize the following using Tabular method $F(A, B, C, D, E) = \sum m(0, 1, 2, 3, 6, 7, 14, 15, 16, 19, 31)$		1
Q3(b)	(i) Reduce the expression $f = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ using K-maps and implement the real minimal expression using NAND logic. (ii) Design the logic circuit for a BCD to decimal decoder.		1

SECTION-C	Attempt <b>ANY ONE</b> following Question	Marks (1X10=10)	CO
Q4(a)	Construct BCD adder using two 4-bit binary parallel adder and logic gates.		2
Q4(b)	Explain 4-bit magnitude comparator.		2



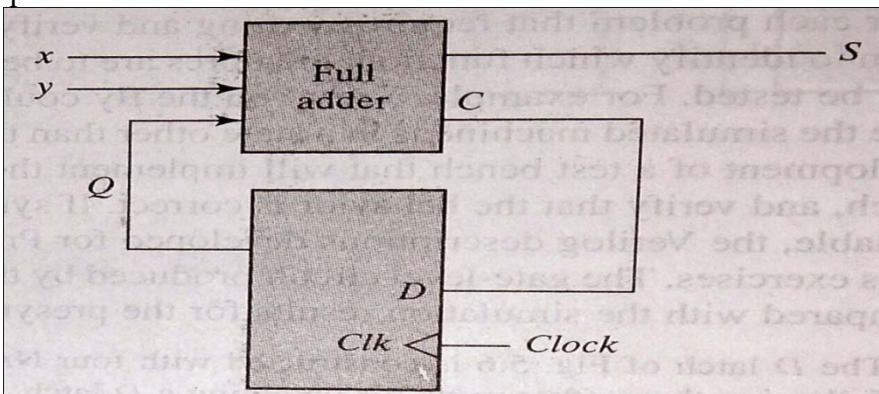
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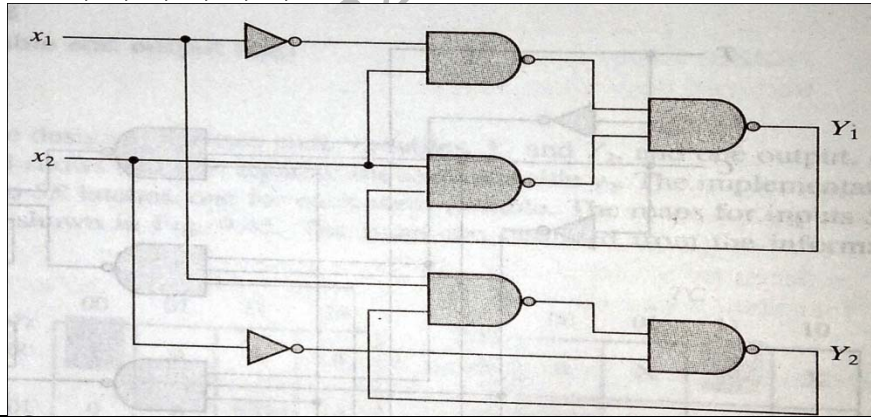
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SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q5(a)	<p>A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in given figure. Derive the state table and state diagram of the sequential circuit. What does this circuit represent?</p> 		3
Q5(b)	Design a 3-bit UP/DOWN counter with a direction control M, using JK flip-flops.		3

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q6(a)	<p>Derive the transition table for the asynchronous sequential circuit shown in given figure. Determine the sequence of internal states <math>Y_1Y_2</math> for the following sequence of inputs <math>x_1x_2</math>: 00,10,11,01,11,10,00.</p> 		4
Q6(b)	<p>(i) Distinguish between static and dynamic hazard. How will you determine hazard in combinational circuits? (ii) Draw the logic diagram of the product-of-sums expression <math>Y = (x_1 + x_2')(x_2 + x_3)</math>. Show that there is a static 0-hazard when <math>x_1</math> and <math>x_3</math> are equal to 0 and <math>x_2</math> goes from 0 to 1. Find a way to remove the hazard by adding one more OR gate.</p>		4

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q7(a)	Design a BCD to Excess-3 code converter and implement it using a suitable PLA.		5
Q7(b)	Draw a neat diagram of TTL NAND gate and explain its operation.		5